Amendments to the Specification:

Please replace the paragraph beginning at page 10, line 20 with the following amended paragraph:

Figure 6 is a block diagram of an instruction request unit 600 according to one embodiment of the present invention. The instruction request unit 600 may look ahead several cycles to determine when the buffers 510, 515 will be emptied so the buffers 510, 515 may be reloaded without any bubbles being introduced into the pipeline in this particular embodiment. The embodiment of the instruction request unit 600 will be described with a cache latency (410, Figure 4) of 2 cycles. Thus, the instruction request unit should look ahead 2 cycles to ensure the buffers 510, 515 are continually reloaded. It can be appreciated that the present invention may be used in a system have a variety of cache latencies, and the instruction request unit 600 would need to look ahead a number of cycles at least equal to the cache latency to ensure no bubbles are inserted. Of course, the instruction request unit 600 may look ahead less than the cache latency. In this embodiment, bubbles may be inserted into the pipeline.

Please replace the paragraph beginning at page 14, line 7 with the following amended paragraph:

The transition block 645 may also determine a buffer 510, 515 is depleted by comparing the most significant bits (MSB) of pointers 655 to the buffers 520-555. For example, each of the 16-bit buffers 520-555 may have an associated pointer. Because there are eight 16-bit buffers, three-bit pointers are used to uniquely identify each buffer. In one embodiment, the buffer 520 has a pointer value of 000, the buffer 525 has a pointer value of 001, the buffer 530 has a pointer value of 010, the buffer 535 has a pointer value of 011, the buffer 540 has a pointer value of 100, the buffer 545 has a pointer value of 101, the buffer 550 has a pointer value of 110, and the buffer 555 has a pointer value of 111. Thus, each of the 16-bits buffers 520, 525, 530, and 535 that comprise the larger buffer 510 have pointer values in which the most significant bit is "0".

Each of the 16-bit buffers 540, 545, 550, and 555 that comprise the larger buffer 515 have pointer values in which the most significant bit is "1".

Please replace the title with the following amended title:

ALIGNING INSTRUCTIONS USING A VARIABLE WIDTH INSTRUCTION ALIGNMENT ENGINE